Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. CLR**
2. **1Q**
3. **1D**
4. **2D**
5. **2Q**
6. **3D**
7. **3Q**
8. **GND**
9. **CLK**
10. **4Q**
11. **4D**
12. **5Q**
13. **5D**
14. **6D**
15. **6Q**
16. **VCC**

**.083”**

**10**

**9**

**8**

**7**

**14 13 12 11**

**15**

**16**

**1**

**2**

**3 4 5 6**

**MASK**

**REF**

**KP-TM9**

**.071”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .005 x .005”**

**Backside Potential: GND or FLOAT**

**Mask Ref: KP-TM9**

**APPROVED BY: DK DIE SIZE .071” X .083” DATE: 5/1/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ALS174**

**DG 10.1.2**

#### Rev B, 7/1